TODO:

* Add transistor to LEDs on V_BIAS and V_RES so they work with voltages lower than their 3V V_F
* Add cap + OR tie to AVDD to STM32 VRES+ pin to extend DAC range to AVDD
* Hook up 74LVC2G157 such that they can be used either in inv/noninv mode or in AND'ing mode
* Switch out driver for PI3HDX12211, add configurable resistors for both pin strapping and I2C options
* Remove clip lines?
* Clean up analog supply/ground — we have a lot of noise there!
* Move STM32 further away from analog frontend
* Make both LVCs voltage controllable by pin strapping (so we can also make the pulse LVC controllable and keep the sampling LVC constant) — fixes ADC alignment problem.
* Check frequency compenstation of sampling opamps — they show some ringing — is this ok?
* Re-consider frontend switching architecture, The mesh flipping is good, I think, but do the termination options make sense?
* Simplify power supply situation. Maybe use a multi-output LDO chip?

High-speed bus muxes

-3dB resistive splitter

Edge → Pulse conversion

Sampling bridge

Sampling bridge

USB 3.0 redriver

Impedances:
25 CM
100 diff
internally terminated

Channel B direction swapped!

Convert to 3V max input levels for RF switches

Noisy high-speed digital stuff and analog switches because I don't trust the charge pumps they might have

General-purpose digital logic

Precision analog stuff (ADC, op-amps)

Isolation measurement bias

RF differential signal bias

LVC delay control supply

TU Darmstadt logo

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